PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	ERIC J. BERGMAN	EXAMINER:	Z. EL-ARINI
APPLICATION NO.:	10/631,376	ART UNIT:	1746
FILED:	JULY 30, 2003	CONF. NO:	2135

FOR: **METHODS OF THINNING A SILICON WAFER USING HF AND OZONE**

DECLARATION OF ERIC J. BERGMAN UNDER 37 C.F.R. 1.132

Mail Stop RCE
Commissioner for Patents
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Sir:

I, Eric J. Bergman, declare:

1. I am the inventor of the methods claimed in Application No. 10/631,376, entitled Methods of Thinning a Silicon Wafer Using HF and Ozone. I have over fifteen years of research and development experience in semiconductor processing. Much of my research and development work has been on ozone-based processing of semiconductor wafers. I am an author of multiple articles in this field. I am employed as a Process Engineer at Semitool, Inc., the Assignee of this Application. I am a named inventor on over 40 U.S. patents and patent applications. Several of these patents and applications relate to processing with ozone.

2. I have reviewed the prior art references cited in the 6/13/06 Final Office Action in connection with the claims in the present application and make the following observations:

3. **The Park Patent** - The Field of the Invention section in Park states the invention relates to "a method for fabricating a semiconductor device and, more particularly, to use of a mixture phase of ozone gas, anhydrous HF gas and deionized water to control the etch selection ratio between oxide film and polysilicon film." Park is very specific that his process is used for the fabrication of a semiconductor device, which reflects a clear intent that his process is used for producing an active electronic circuit.

In other words, Park is not directed to thinning a wafer or a semiconductor substrate (the substrate being the platform on which the semiconductor device is formed, as opposed to the actual active circuit itself). Indeed, Park discloses a method for fabricating a semiconductor device, not for etching a semiconductor wafer. Even where the substrate is incorporated into the actual device through the formation of transistor regions in the substrate, this only incorporates the top few-hundred angstroms of the substrate into the device. The remaining material is not part of the device, and, in fact, is generally considered detrimental to the device, which is why as much of this material as possible is typically removed prior to packaging.

Wafer thinning occurs at only two times in the life of a wafer: (1) during the manufacture of the wafer before any device structure is formed on the wafer - this is done to bring the substrate material into specification for thickness and surface

finish; and (2) after all device fabrication has been completed. The wafer is thinned in order to make dicing of the wafer easier and to optimize packaging of the finished device. The wafer is most commonly single-crystal silicon. It may be GaAs or some other III-V compound, but it is never polysilicon. Persons skilled in semiconductor device manufacturing recognize that "etching" does not imply "thinning" of the substrate. A polysilicon etch implies that thinning of the single-crystal silicon substrate is not an objective and is not performed.

In Park, the objective is to etch a thermal oxide- and polysilicon-exposed wafer. Thus, Park deals with wafers having both exposed oxide and exposed polysilicon. Park describes having a low etch selectivity between a silicon oxide film and polysilicon, which is important only if both films are simultaneously exposed. Both of these films would be present only during device fabrication, which indicates that Park is performing a pattern etch, not a wafer-thinning operation. The possibility that a minimal amount of wafer substrate material might be consumed during the etching process is not an objective, but a potential side-effect. However, Park, by stating that his process is to be used to etch polysilicon and oxide, specifically implies that the single-crystal substrate (i.e., the wafer) would not be etched to a significant degree, since the single-crystal silicon substrate would not have polysilicon and silicon oxide simultaneously exposed.

Park envisions his process to be used for forming the active region of the device. He intends to simultaneously etch polysilicon and silicon oxide at a low selectivity in order to retain the physical dimensions of the structure. In my 21 years of experience in the semiconductor industry, I have never encountered a polysilicon

substrate for semiconductor device fabrication. In device fabrication, I have etched silicon, polysilicon, silicon dioxide, silicon nitride, aluminum, tungsten, cobalt, nickel, platinum, gold, numerous silicides, and various other exotic films, such as hafnium oxides. All of these were etch processes. None of these are done with the intent of thinning the wafer, because thinning a wafer is not consistent with device fabrication as in Park.

4. **The EP '177 Patent** - The EP '177 patent teaches removing an oxide film from a semiconductor wafer. EP '177 lists ozone in passing as one of several different gases that may be used. However, the EP '177 process is performed using HF gas. The top of page 4 of EP '177 discusses preventing undesirable oxidation of the etched silicon surface, and avoiding use of water having dissolved ozone to avoid oxidation. Logically, ozone, which is an even stronger oxidizer, should also be avoided, based on this content of EP '177. On the other hand, the process in the claims of my application include use of ozone.

5. **Combination of Park and EP '177**

The EP '177 patent discloses etching a silicon dioxide film (not the wafer substrate) to minimize oxygen on the wafer surface. Park discloses a low selectivity etch of silicon oxide and polysilicon by using HF gas, ozone gas, and water vapor. If these two patents are combined, the result is a method for removing silicon dioxide and polysilicon using anhydrous HF and ozone with water vapor, followed by a rinse which may use anhydrous HF and ozone. There is still nothing there in the combination to reasonably instruct thinning a wafer.

There is also nothing in the combination relevant to the etch rates described in claims in my application. The etch rate taught by Park is simply a number. Park shows four graphs and two tables. None of these contain any silicon or polysilicon etch rate data. The only silicon or polysilicon data in these graphs and tables are from conventional aqueous HF or BOE processes. The data that Park provides in the body of his patent, indicating a polysilicon etch rate of up to 50A/sec, cannot be applied to single-crystal silicon, which generally etches very differently from polysilicon. There is simply no way to combine the teachings of Park with the teachings of EP '177 to obtain the process of my application, particularly since neither

I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 under Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: Sept. 8, 2006

Eric J. Bergman